A 0.18μm 3.25-5.6GHz and 6-10.4GHz Band Switchable Low Noise Amplifier

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***Abstract*— One band switchable low noise amplifier (LNA) is designed for wideband applications. The proposed band switchable LNA has two switchable bands. The design consists of a input matching circuit, two cascode common-source amplifiers and an output buffer for measurement. The proposed LNA is designed with two switching capacitors as loading that use NMOS to make high quality factor. The proposed LNA gives switchable gains of 10.8dB and 16.8dB, and noise figure of 3.6-6.2dB and 3.1-6.5dB at 3.25-5.6GHz and 6-10.4GHz frequency band, respectively, while consuming 22.46mW through a 1.8V power supply using the TSMC 0.18μm CMOS technology.**

***Index Terms*— LNA, low noise amplifier, band switchable, switching capacitors, CMOS, RF.**

I. Introduction

UWB is a popular technology since it can achieve a high data rate with relatively low power. MB-OFDM is a popular UWB technique proposed by Intel. To avoid interference with U-NII band (5GHz-6GHz) in some countries, MB-OFDM divides the whole bandwidth into several groups, *i.e.* Group 1 (3.1GHz-5GHz), Group 2 (5GHz-6GHz), and Groups 3-5 (6GHz-10.6GHz). To reduce cost, a band switchable RF is preferred, *i.e.* switching for 3.1GHz-5GHz and 6GHz-10.6GHz bands.

There were several UWB LNA proposals, *e.g.* see [3][4][5][6]. There were several interesting wideband input impedance matching solutions. In [9], the authors proposed a broadband input matching circuit. This design requires accurate transformer parameters but the standard devices of TSMC 0.18μm does not include the transformer parameters. In [7], the authors proposed a graph-based technique for input matching. However the design used four inductors for input matching and five inductors for output matching, which costs a lot of area. In [1], the input matching circuit of this wideband LNA design is actually the Chebyshev filter. Although this design can also be used as an input matching circuit, it requires four inductors.

In UWB, we need to avoid bandwidth overlapping. There are two solutions to achieve this goal. One is using switching band, and another is using notch filter [10]. Because the quality factor (Q) implemented in integrated circuit (IC) is in general low, the notch filter in IC does not have sufficient high Q for wideband design. Although in [10], the authors used active notch filter to avoid low Q, the design demanded more power. For switching band, it needs fewer devices than the notch filter and the noise of the out-off bands can be removed because we do not use two bands simultaneously. Various types of switches for switching band LNA were proposed. In [11], the authors used PMOS as a switch in the load of LNA. The mobility of PMOS is lower than that of NMOS. Thus, its turn-on resistance is large, which leads to a low Q and a low gain. In [13], the authors proposed to use NMOS-based switch. In [12], the authors changed the passive device value by a switching inductor to achieve high gain.

In this paper, we use switching capacitor to implement the band switchable LNA. We use NMOS to realize the switching capacitor because its turn-on resistance (r_{on}) is lower than that of PMOS. The low r_{on} makes the NMOS more like an ideal switch than PMOS. Thus we can obtain higher Q. The higher the Q is, the higher gain we can obtain. We also use large resistor to reduce the parasitic capacitance of the switch. Hence the size of the switch can be increased so that r_{on} can be decreased. As a result we can obtain higher gain. Moreover the proposed design contains a conventional source-degeneration input matching, an inductor shunted in the input RF path and a capacitor connected with input the RF path [1]. It is worthy to emphasize that the proposed design does not need exact transformer parameters and the number of inductors is one fewer than the Chebyshev filter.

II. Proposed Switching Capacitor

Compared to the scheme in [11], the proposed switching capacitor amplifier replaces the PMOS with a NMOS and adds a resistor R_1 as shown in Fig. 1(a). The reasons are as follows: First since NMOS has lower r_{on} than PMOS, NMOS has larger gain than PMOS when it is on. Hence we use the NMOS as switch. Second, the added large resistor (R_1) can reduce the parasitic capacitance. If we do not have R_1, the equivalent capacitance, C_{eq}, is that C_1 series C_{gs} when the switch is off. On the other hand, if we have R_1, C_{eq} is that C_{gs} and C_{gd} series C_1 and C_2 when the switch is off. Hence with R_1 the parasitic capacitance is reduced from C_{gs} to that C_{gs} series C_{gd}.

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Due to the reduction of the parasitic capacitance, the size of the NMOS can be increased, which leads to a decreased r_{on}. Therefore the gain is increased when the switch is on.

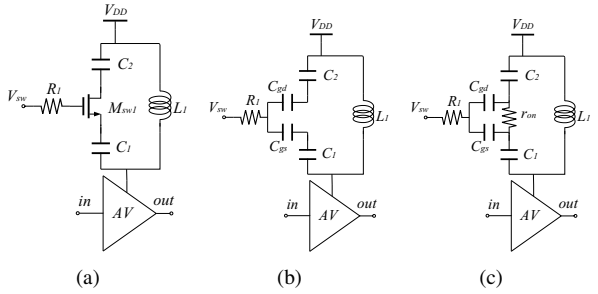

Fig. 1. The proposed switching capacitor amplifier: (a) The proposed circuit. (b) When M_{sw1} is off. (c) When M_{sw1} is on.

Fig. 1(a) and Fig. 1(b) shows the situation when the NMOS M_{sw1} is turned off. Due to the adding of R_1, C_{eq} is the parasitic capacitance in M_{sw1}, *i.e.* C_{gs} and C_{gd} series C_1 and C_2. By designing that $C_1, C_2 \gg C_{gs}, C_{gd}$, C_{eq} is that C_{gs} series C_{gd}, *i.e.*, $C_{eq} = C_{gs}C_{gd}/(C_{gs}+C_{gd})$. Fig. 1(c) shows M_{sw1} is turned on. Then, C_{eq} is that r_{on} series C_1 and C_2. Thanks to the use of the NMOS, r_{on} has low resistance. Moreover, the use of R_1 can further increase the size of NMOS, which leads to a lower resistance. Because r_{on} has low resistance, r_{on} can be neglected. Hence the equivalent capacitance is $C_{eq} = C_1C_2/(C_1 + C_2)$. Therefore the circuit can satisfy the resonance of the load at two different frequencies by turning on or turning off M_{sw1}. The resonant frequency is $\omega = 1/\sqrt{L_1C_{eq}}$. The size of M_{sw1} trades off between C_{gs}, C_{gd} and r_{on}.

III. Proposed band switchable LNA

The proposed band switchable LNA is shown in Fig.2, which consists of an input matching network that is implemented by the Butterworth Filter [1] (consisting of L_d, L_g, L_s, C_c and C_{gs1}); a two-stage cascaded cascode-amplifier (containing M_1, M_2, M_3, and M_4); a switch capacitance loading of the amplifiers (consisting of L_1, L_2, M_{sw1}, C_3, C_4 and M_{sw2}); an output buffer (consisting of M_6 and M_7); three DC blocking capacitors (consisting of C_b); three RF chocks (consisting of R_1, R_2 and R_b). V_{sw1} and V_{sw2} are the control voltage source of the proposed switching capacitor loading. When V_{sw1} and V_{sw2} are 1.8V, it is in the low band mode (3.25-5.6GHz). On the contrary when both the voltages are 0V, it is in the high band mode (6-10.4GHz). In high band mode, we can achieve a given frequency by letting M_{sw1} and M_{sw2} off, and then adjusting the sizes of these two transistors. In low band mode, we let M_{sw1} and M_{sw2} on and the sizes of M_{sw1} and M_{sw2} will affect the resistance of the proposed switching capacitor loading. Consequently, it affects the gain. Please note that the size of M_1 trades off between the input matching and the noise figure of the LNA.

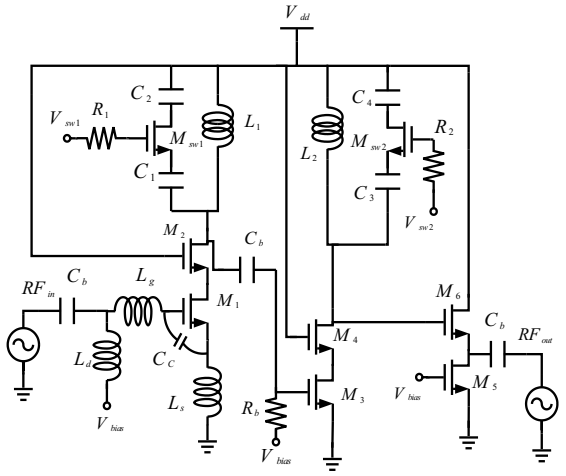

Fig. 2. The proposed band switchable low noise amplifier.

A. Wideband Input Matching

We use the input matching scheme shown in Fig. 3 [1]. In high frequency the inductor shunts with input RF path,

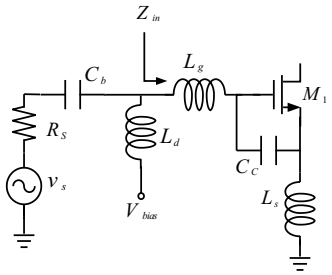

Fig. 3. The input matching for UWB LNA.

i.e. L_d, is approximately open. Hence the circuit acts like an inductive source degeneration circuit. The equivalent capacitance is the series connection of $(C_{gs}+C_c)$ and C_b. Hence the input impedance is expressed as

$$s(L_g + L_s) + \frac{1}{s((C_{gs}C_b + C_cC_b)/(C_{gs} + C_c + C_b))} + \omega_T L_s,$$

where $\omega_T L_s$ is set to be 50 ohm. The resonance frequency for high frequency is

$$\omega = \sqrt{\frac{1}{(L_g + L_s)((C_{gs}C_b + C_cC_b)/(C_{gs} + C_c + C_b))}}. \quad (1)$$

For low frequency, the input impedance is expressed as

$$Z_{in} = \frac{1}{sC_b} + \left[sL_d // \left(sL + \frac{1}{sC} + R\right)\right]. \quad (2)$$

where $L = L_g + L_s$, $C = C_{gs} + C_c$ and $R = g_m L_s/C_{gs}$. Then we can design the impedance in Eq.(2) to be 50 ohm.

B. Cascoded Amplifier with LC-Tank Load

In the proposed scheme, no matter the switch is on or off, the load of LNA acts like an LC-tank. The cascode amplifier with LC-tank can reduce the Miller effect on input transistors M_1 and M_3 in Fig.2 and thus it improves

high-frequency performance. Please note that the LC-Tank Load is usually used in narrow-band systems due to its prominent frequency-selective characteristics.

C. Cascade Amplifier with LC-Tank Load

In the cascade circuit, the first-stage amplifier with the load realized by LC-tank contributes the gain for lower frequency. The second-stage amplifier contributes the gain for higher frequency. Thus, the wide bandwidth and high power gain can be achieved.

IV. Experimental result

The measurement results of the proposed band switchable wideband LNA use the 4-Port Network Analyzer (Agilent 5230A), Noise Figure Analyzer (Agilent N8975A) and Signal Generator (Agilent E8247C) that supported by the National Chip Implementation Center (CIC) [8]. The simulation results use the Agilent Advance Design System (ADS) 2006A simulator. The microphotograph of the band switchable wideband LNA is shown in Fig. 4, which was fabricated in the TSMC 0.18μm CMOS process technology. The die area is 1.15mm$\times$1.02mm with bonding pads. The low band mode and high band mode

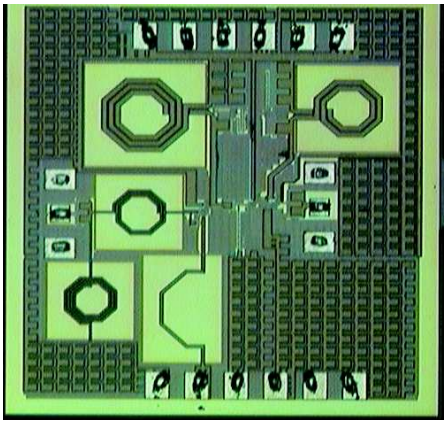

Fig. 4. The chip photo of band switchable wideband LNA.

measurement results are shown as follows: Figs. 5-7 are S-parameters, S_{11}, S_{21} and S_{22}, respectively. S_{11} is lower than -9.6dB at low band and lower than -10.8dB at high band. S_{21} has maximum power gain 10.8dB for low band and 16.8dB for high band. S_{22} is lower than -8.4dB at low band and lower than -10.4dB at high band. Fig. 8 shows that the noise figure is 3.6-6.2dB for low band and 3.1-6.5dB for high band, respectively. Fig. 9 shows that the IIP_3 is -11dBm for low band and -16dBm for high band, respectively. Finally the results are summarized in Tab. I. The total power of measurement passes through a 1.8 V power supply is 22.46mW. The comparison is shown in Tab. II. The power consumption of the proposed LNA is lower than other schemes. The noise figure is lower than [5]. The gain is higher than [5].

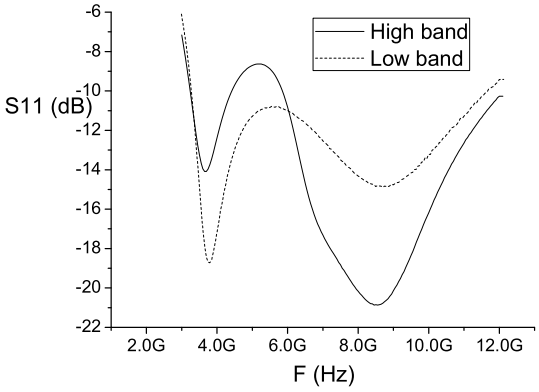

Fig. 5. The S_{11} parameter of band switchable wideband LNA.

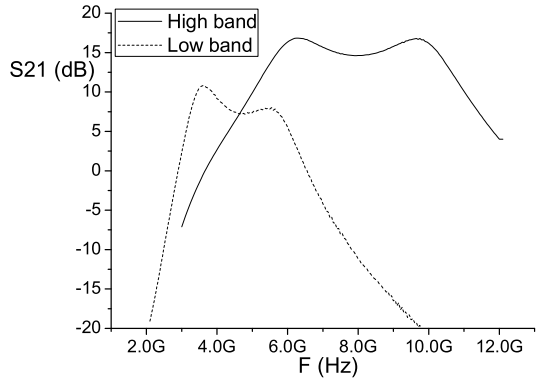

Fig. 6. The S_{21} parameter of band switchable wideband LNA.

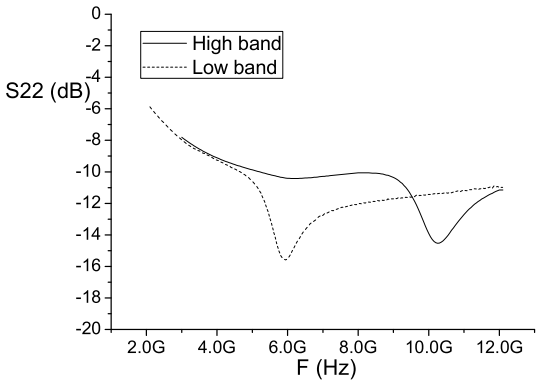

Fig. 7. The S_{22} parameter of band switchable wideband LNA.

V. Conclusion

In this paper, we proposed a band switchable LNA for wideband application, which gives gain of 10.8dB/16.8dB, and noise figure of 3.6-6.2dB/3.1-6.5dB at 3.25-5.6GHz/6-

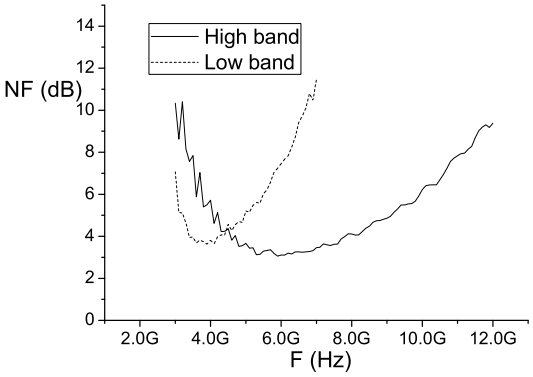

Fig. 8. The NF parameter of band switchable wideband LNA.

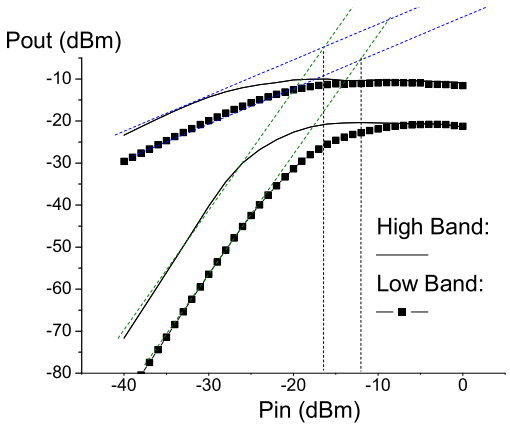

Fig. 9. The IIP_3 parameter of band switchable wideband LNA.

10.4GHz frequency band, respectively. It consumes 22.46mW through a 1.8V power supply using the TSMC 0.18μm CMOS technology. Under the same power consumption, the proposed LNA has higher gain than [13]. For similar gain level, the proposed LNA consumes lower power than [4], [5] and [10]. Compared to [6], the proposed LNA has higher gain as well as lower power.

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REFERENCES

[1] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," IEEE JSSC, Dec 2004.
[2] FCC, "Final Rule of the Federal Communications Commission, 47 CFR Part 15, Sec. 503," Federal Register, May 2002.
[3] H. Zhang, X. Fan, E.S. Sinencio, "A Low-Power, Linearized, Ultra-Wideband LNA Design Technique," IEEE JSSC, Feb. 2009.

TABLE I

MEASUREMENT RESULT OF PROPOSED WIDEBAND LNA.

Technology	TSMC 0.18um	
Topology	Switch-Capacitor	
Specification	Low	High
Supply Voltage	1.8 V	1.8 V
S_{11}	< -9.6 dB	<-10.8 dB
S_{22}	< -8.4 dB	< -10.4 dB
Power Gain	7.5dB - 10.8dB	13.8dB - 16.8dB
NF	3.6dB - 6.2dB	3.1dB - 6.5dB
P_{1dB}	-22 dBm	-25 dBm
IIP_3	-11 dBm	-16 dBm
BW(GHz)	3.25-5.6	6-10.4
Power	22.46 mW	22.46 mW

TABLE II

PERFORMANCE COMPARISON OF VARIOUS BAND SWITCHABLE WIDEBAND LNAS

Paper	Topology	Technology	BW (GHz)	S_{11} (dB)	S_{22} (dB)	S_{21} (dB)	NF (dB)	Power (mW)
This work	Switch Cap.	CMOS 0.18 um	3.25-5.6	<-9.6	<-8.4	7.5-10.8	3.6-6.2	22.46
			6-10.4	<-10.8	<-10.4	13.8-16.8	3.1-6.5	22.46
[13]◎	Switch Cap.	CMOS 0.18 um	3.1-4.8	<-8.9	<-8.3	5.6-8.4	4.1-4.9	24.8
			6-8.1	<-9.4	<-9.7	9-11.1	3.8-4.1	24.8
			8.1-10.3	<-8.4	<-10.1	8.1-10.3	4.1-4.8	24.8
[10]	Notch Filter	CMOS 0.13 um	3-5	<-10	N/A	19.4¥	3.5*	31.5
[4]	4-stages common-source	CMOS 0.18 um	3-10.6	<-9	<-13	15.9-17.5	3.1-5.7	33.2
[5]	3-stages common-source	CMOS 0.18 um	3-6	<-12.2	<-10.1	13.5-15.8	4.7-6.7	59.4
[6]	Cascode	UMC 0.13 um	2.2-9	<-9.2	<-10	11.3	3.9-4.6	30

◎－Simulation result ¥－Maximum voltage gain *－minimum NF Cap: capacitor

[4] Y. Lu, K. S. Yeo, A. Cabuk, J. Ma, M. A. Do and Z. Lu, "A novel CMOS low noise amplifier for 3.1 to 10.6GHz ultra wide band wireless receivers," IEEE Trans. CAS, Aug. 2006.
[5] C.-P. Chang and H.-R.Chuang, "0.18 um 3-6 GHz CMOS broadband LNA for UWB radio", Electronics Letters, Jun. 2005.
[6] G.D. Nguyen, K. Cimino and M. Feng, "A RF CMOS amplifier with optimized gain, noise, linearity and return losses for UWB applications," IEEE RFIC, Jun. 2008.
[7] G.D. Nguyen,K. Cimino and M. Feng,"A RF CMOS amplifier with optimized gain, noise, linearity and return losses for UWB applications," IEEE RFIC, Jun. 2008.
[8] http://www.cic.org.tw.
[9] C.-T. Fu and C.-N. Kuo, "3-11 GHz CMOS UWB LNA using dual feedback for broadband matching," IEEE RFIC, Jun. 2006.
[10] A. Bevilacqua, A. Vallese, C. Sandner, M. Tiebout, A. Gerosa and A. Neviani, "0.13um CMOS LNA with integrated balun and notch filter for 3-to-5GHz UWB receivers," IEEE ISSCC, Feb. 2007.
[11] S. H. M. Lavasani, B. Chaudhuri and S. Kiaei, "A pseudo-concurrent 0.18um multi-band CMOS LNA," IEEE RFIC, Jun. 2003.
[12] T. K. K. Tsang and M. N. El-Gamal, "Dual-band sub-1v CMOS LNA for 802.11a/b wlan applications," IEEE ISCAS, May. 2003.
[13] Z.-Y. Huang, C.-C. Huang, C.-C. Chen and C.-C. Hung, "CMOS low-noise amplifier with switching groups for MB-OFDM UWB wireless radio system," IEEE ICUWB, Sep. 2007.