VLSI Implementation of a Low Complexity 4x4 MIMO Sphere Decoder with Table Enumeration

Kai-Jiun Yang*, Shang-Ho Tsai*, Ruei-Ching Chang*, Yan-Cheng Chen* and Gene C.-H. Chuang†
* Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan
† Information and Communications Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan

***Abstract*— In this work a sphere decoder with low complexity is proposed and implemented. We propose a simplified norm algorithm, which is called admissible set elimination (ASE), to dramatically decrease the number of searching nodes. In addition, the decoder uses table-look-up to acquire the enumeration order of different constellations. As a result, the critical path is shortened and the throughput is enhanced. Compared to the optimal ML detector, the proposed scheme greatly improves the complexity and throughput, while the performance only degrades around 0.5 dB. The proposed scheme is fabricated by a TSMC 90 nm process. The area is 0.85 mm^2, and the average throughput can be up to 411.3 Mbps when the clock rate is 108.7 MHz.**

I. Introduction

Multiple-input multiple-output (MIMO) systems provide significant advantages such as spatial multiplexing and diversity, and have been applied in several communication standards including IEEE 802.11x, Wi-Fi LAN, and 4G WAN such as LTE or IEEE 802.16x. The data rate can be greatly boosted by increasing the number of data streams and the modulation levels. The detection complexity, however, also increases exponentially as these parameters grow.

The detecting algorithms for MIMO systems have been classified into linear and non-linear detection. Zero-forcing (ZF) and minimum mean-squared error (MMSE) are both linear detection, which estimate the information about channel matrix and try to compensate for channel effect. The linear detection methods have low computational complexity but suffer from extreme performance-loss because they cannot fully remove interference caused by the channel. Maximum likelihood detection (ML) and successive interference cancelation (SIC) are considered to be non-linear detection. The ML detector is optimal in terms of performance [1], but the complexity surges exponentially as the number of data stream increases because it is based on exhaustive search. To overcome these issues, previous works have proposed a variety of sphere decoding (SD) algorithms, such as K-best [2]- [4] and depth-first [5], [6]. The main drawback of the depth-first algorithm is the dramatic variation of its search time, which may be impractical to use in a real-time manner. On the other hand, the K-best sphere decoding (KSD) has fixed throughput, which uses breath-first search [7]. However, the value K in KSD needs to be sufficiently large to achieve comparable performance of the ML detector, which again leads to high complexity and power consumption. K-best and set-elimination (SE) were combined in [2] and, at most, K nodes were considered with smallest partial Euclidean distance (PED) in each level. Such a combination can achieve higher throughput. The authors in [3] propose a new architecture which can support QPSK, 16-QAM, and 64-QAM, but they deem all the modulations to be 64-QAM. A K-best with K=5 was implemented via VLSI design in [4]. The algorithms in [5] and [6] use depth-first sphere-decoding but only support 16-QAM modulation. The above proposals reduce the decoding complexity at the price of compromised performance. The hardware implementation is still challenging for higher M-ary modulations.

In this paper we propose a pre-filtering scheme called admissible set elimination (ASE). The proposed ASE can eliminate the candidate nodes by ranging real and imaginary parts separately. As a result, the number of nodes to be evaluated can be dramatically decreased. In addition, by using the proposed ASE together with table enumeration [8], the number of visiting nodes and the computational time of the critical path can be greatly decreased. This results in an improved throughput. The proposed architecture can support BPSK, QPSK, 16-QAM and 64-QAM and was fabricated by a TSMC 90 nm process. The average data rate is 411.3 Mbps when the clock rate is 108.7 MHz.

II. System Model and Sphere Decoding

Let us consider the MIMO system with M_T and M_R receive antennas. The $M_R \times 1$ received vector can be expressed as

$$\mathbf{y} = \mathbf{H}\mathbf{s} + \mathbf{n}, \tag{1}$$

where $\mathbf{H}$ is a $M_R \times M_T$ channel matrix, $\mathbf{s}$ is a $M_T \times 1$ transmit vector, where each element is of q bits, and $\mathbf{n}$ is a $M_R \times 1$ i.i.d. complex Gaussian noise vector. Assume that $\mathbf{H}$ is known to the receiver, and $M_R \geq M_T$. Each q-bit entry in $\mathbf{s}$ is mapped into an M-QAM symbol, where $2^q = M$.

A. Maximum Likelihood Detection and Sphere Decoding

The ML detection searches all the transmitted symbol $\mathbf{s}_{ML}$ and selects the one which satisfies

$$\mathbf{s}_{ML} = \arg \min_{\mathbf{s} \in \mathcal{O}^{M_T}} \|\mathbf{y} - \mathbf{H}\mathbf{s}\|^2, \tag{2}$$

where $\mathcal{O}^{M_T}$ denotes all possible transmitted symbol vectors spanned by M-QAM constellation. The computational complexity of the ML detection grows exponentially with the size of constellation and the lattice dimension. This drawback makes it impractical to be realized physically.

978-1-4673-5762-3/13/$31.00 ©2013 IEEE

Sphere decoding (SD) algorithm is a simplified ML detection, and it searches only the vectors $\mathbf{Hs}$ within a hypersphere with radius r centered at received $\mathbf{y}$, examining $\mathbf{s}$ that satisfy

$$\|\mathbf{y} - \mathbf{Hs}\|^2 < r^2. \tag{3}$$

Additionally, the channel matrix $\mathbf{H}$ can be decomposed using the QR factorization: $\mathbf{H} = \mathbf{QR} = [\mathbf{Q}_1\ \mathbf{Q}_2][\mathbf{R}_1\ \mathbf{0}]^T$ where $\mathbf{R}_1$ is an $M_T \times M_T$ upper triangular matrix, $\mathbf{0}$ is an $(M_R - M_T) \times M_T$ zero matrix, and $\mathbf{Q}$ is an $M_R \times M_R$ unitary matrix. Letting $\widehat{\mathbf{y}} = {\mathbf{Q}_1}^H \mathbf{y}$, (2) can be rewritten as

$$\mathbf{s}_{ML} = \arg \min_{\mathbf{s} \in \mathcal{O}^{M_T}} \sum_{i=1}^{M_T} |\widehat{y}_i - \sum_{j=i}^{M_T} R_{ij} s_j|^2, \tag{4}$$

Starting from the last element $i = M_T$ in $\mathbf{s}_{ML}$, the decoding process recursively finds the shortest path with the minimum partial Euclidean Distances (PEDs). The PEDs $X_i(\mathbf{s}^{(i)})$ are calculated by

$$X_i(\mathbf{s}^{(i)}) = X_{i+1}(\mathbf{s}^{(i+1)}) + |e_i(\mathbf{s}^{(i)})|^2, \tag{5}$$

where $i = 1,\ 2,\ \ldots,\ M_T$ and

$$|e_i(\mathbf{s}^{(i)})|^2 = |(\widehat{y}_i - \sum_{j=i+1}^{M_T} R_{ij} s_j) - R_{ii} s_i|^2. \tag{6}$$

The traverse can be reduced because the current PED includes the PED from the previous search. Moreover, if the calculating PED is larger than the search radius r, the following traverses are terminated since the PEDs must be outside the hypersphere. As a result, the initial radius is set to infinity to alleviate the problem of initial radius choice [5]. Once the leaf in the branch is reached, the radius is updated with that PED.

B. Table Enumeration

The enumeration of M-ary constellation points is another important means in improving the searching speed. An efficient order not only finds the minimal PED in time but also curtails the critical paths in hardware design. The key point of the design is the enumeration of the sibling nodes which are the other candidates with fairly close PEDs. Schnorr and Euchner (SE) traverse the candidate in ascending order of the corresponding PEDs [7]. For 2^q candidates, q levels of comparisons for sorting are required, which can be the bottleneck of the throughput.

To avoid real-time sorting, the authors in [8] proposed a table enumeration method. This method divides the constellation plane into finite regions. Each region has its own enumeration order based on the distance from the center of the region to all possible constellation points. Note that the distance is acquired off-line and the subsequent orders are stored in a table. When performing sphere decoding, the order to evaluate $\mathbf{s}$ is determined by table look-up directly. With a reasonable performance loss, this method can reduce complexity because it does not need to calculate the PEDs.

III. Proposed Method

This work proposes a simplified norm algorithm to find the PEDs, and eliminating irrelevant nodes at early stage. Additionally the candidate nodes are enumerated based on the off-line calculated orders kept in a look-up table. The proposed scheme not only increases the throughput but also shorten the critical paths in circuitry.

A. Admissible Set Elimination (ASE)

The PED can be approximated by l^1-norm. Burg *et al.* approximated l^2-norm by means of a simplified norm algorithm such as l^1- or l^∞-norm to reduce the complexity [5]: Using l^1-norm approximation has better performance than that of using l^∞-norm approximation, because the residual radius $\|\mathbf{y} - \mathbf{Hs}\|$ satisfies $\|\mathbf{y} - \mathbf{Hs}\|_\infty \leq \|\mathbf{y} - \mathbf{Hs}\| \leq \|\mathbf{y} - \mathbf{Hs}\|_1$. As a result the PED in (5) can be approximated as

$$\begin{aligned} X_i(\mathbf{s}^{(i)}) &\approx |X_{i+1}(\mathbf{s}^{(i+1)})| + |e_i(\mathbf{s}^{(i)})| \\ &\approx \max(|X_{i+1}(\mathbf{s}^{(i+1)})|, |e_i(\mathbf{s}^{(i)})|), \end{aligned} \tag{7}$$

where $|e_i(\mathbf{s}^{(i)})|$ may be approximated as

$$\begin{aligned} |e_i(\mathbf{s}^{(i)})| &\approx |\Re\{e_i(\mathbf{s}^{(i)})\}| + |\Im\{e_i(\mathbf{s}^{(i)})\}| \\ &\approx \max(|\Re\{e_i(\mathbf{s}^{(i)})\}|, |\Im\{e_i(\mathbf{s}^{(i)})\}|). \end{aligned} \tag{8}$$

Using (7), the hypersphere criterion in (3) may be consequently approximated as $|X_{i+1}(\mathbf{s}^{(i+1)})| + |e_i(\mathbf{s}^{(i)})| < r$, which means $|e_i(\mathbf{s}^{(i)})| < r$. Thus, (6) can be approximated as

$$|e_i(\mathbf{s}^{(i)})| = |b_{i+1} - R_{ii} s_i| < r, \tag{9}$$

where $b_{i+1} = (\widehat{y}_i - \sum_{j=i+1}^{M_T} R_{ij} s_j)$. Note that (8) suggests the computation can be processed as real part and imaginary part individually. In such a case, (9) can be rewritten as $-r < \Re\{(b_{i+1} - R_{ii} s_i)\} < r$ and $-r < \Im\{(b_{i+1} - R_{ii} s_i)\} < r$. After the QR decomposition, the image part of R_{ii} is zero. As a result the candidates of $\mathbf{s}_i$ can be limited within

$$\begin{aligned} -r + \Re\{b_{i+1}\} < R_{ii}\Re\{s_i\} < r + \Re\{b_{i+1}\} \\ -r + \Im\{b_{i+1}\} < R_{ii}\Im\{s_i\} < r + \Im\{b_{i+1}\}. \end{aligned} \tag{10}$$

Take a 3×3 MIMO system with 64-QAM modulation for instance. Let $r = 3$, $\widehat{\mathbf{y}} = (6.12 - 5.04j\ -15.60 + 18.86j\ 6.12 - 5.04j)^T$, $(R_{11}\ R_{22}\ R_{33}) = (1.31\ -3.11\ 1.62)$, $(R_{12}\ R_{23}) = (-0.77 - 0.21j\ \ 1.06 - 0.03j)$ and $R_{13} = 0.25 + 0.24j$, the possible $\mathbf{s}$ are $s_3 = 7 - 3j$ or $7 - 5j$, $s_2 = 7 - 7j$, and $s_1 = 7 - 5j$ or $7 - 7j$. The visited nodes are reduced from 64^3 to 5, which is a huge reduction.

B. Finite Search with Enumeration Table

Using look-up-table (LUT) to search sibling nodes avoids a series of comparison [8]. This becomes more pronounced for large M-ary QAM. The design challenge lies in finding the balance between the resolution and throughput, where granularity in dividing the sub-region and the computing complexity form the trade-off.

Let us continue with our proposed ASE. In layer i, assume the searching for the best constellation points has been done, and each quantized result satisfies (10). The proposed scheme

TABLE I

THE ENUMERATING ORDER FOR EACH SUB-REGION IN 16-QAM.

Region	Enumerating Order
1	7, 11, 6, 10, 8, 3, 12, 2, 4, 15, 5, 9, 14, 16, 1, 13
2	7, 3, 6, 2, 8, 11, 4, 10, 12, 5, 1, 9, 15, 14, 16, 13
3	7, 8, 11, 12, 3, 6, 4, 10, 15, 2, 16, 14, 5, 9, 1, 13
4	7, 8, 3, 4, 11, 6, 12, 2, 10, 15, 5, 16, 1, 9, 14, 13
5	3, 7, 2, 6, 4, 8, 11, 1, 5, 10, 12, 9, 15, 14, 16, 13
6	3, 2, 7, 4, 6, 8, 1, 5, 11, 10, 12, 9, 15, 14, 16, 13
7	3, 7, 4, 8, 2, 6, 11, 12, 10, 1, 5, 15, 16, 9, 14, 13
8	3, 4, 7, 2, 8, 6, 11, 1, 12, 5, 10, 9, 15, 16, 14, 13
9	8, 12, 7, 4, 11, 3, 16, 15, 6, 10, 2, 14, 5, 9, 1, 13
10	8, 7, 4, 3, 12, 11, 6, 2, 10, 16, 15, 5, 1, 14, 9, 13
11	8, 12, 7, 4, 11, 3, 16, 15, 6, 10, 2, 14, 5, 9, 1, 13
12	8, 4, 7, 12, 3, 11, 16, 6, 2, 15, 10, 14, 5, 1, 9, 13
13	4, 8, 3, 7, 12, 2, 11, 6, 10, 16, 1, 15, 5, 9, 14, 13
14	4, 3, 8, 7, 2, 6, 12, 11, 1, 10, 5, 16, 15, 9, 14, 13
15	4, 8, 3, 7, 12, 11, 2, 6, 16, 10, 15, 1, 5, 14, 9, 13
16	4, 8, 3, 7, 12, 2, 11, 6, 10, 16, 1, 15, 5, 9, 14, 13

divides the plane into 4 sub-regions. Comparing with the resolution of 8 sub-regions and that of 16 sub-regions, the division of 4 sub-regions saves memory by 50% and 75%, respectively. Moreover, the decoding process is much easier and the performance is satisfactory if the proposed ASE is used. Therefore 4 sub-regions division with the proposed ASE is chosen for implementation.

Take 16-QAM modulation for instance, the whole complex plane for 16-QAM is divided into 64 sub-regions as shown in Fig. 1. Each of the 64 sub-regions has a off-line computed decoding order as tabulated in Tab. I. This table is obtained by enumerating the constellation points in ascending PEDs from the centers of each sub-regions to all the constellation points. Since the second to the fourth quadrants are symmetric to the first quadrant, the same table can be applied by simple transformation. Consequently, for M-ary QAM modulation only M-entry table is required thanks to the symmetry.

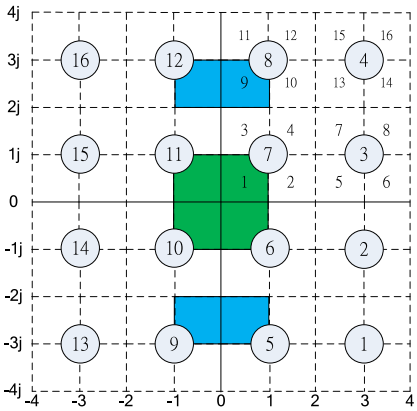

Fig. 1. Finite region division for 16-QAM. Since the coordinates are symmetric, only the first quadrant is labeled.

IV. VLSI IMPLEMENTATION AND PERFORMANCE

A. Algorithm Evaluation

Initially the radius is chosen by zero-forcing. Since searching via LUT may skip the global optimal solution and stick in a local optimal solution in some cases, it is recommended that the root node has been visited at least K times to ensure not falling into a local optimal solution. By extensive simulation on a 4×4 sphere decoding, it is found that a suitable value for K is 7. It is comprehensible that the performance of 4 sub-regions division is not as good as that of 8 or 16 sub-regions division. Still simulated annealing evaluation provides practical references for the actual design if K is set to be 7 for 4 sub-regions division. The performance of the proposed method for 64-QAM with $K = 7$ is as shown in Fig. 2. Observe that it only degrades around 0.5dB compared with the ML solution.

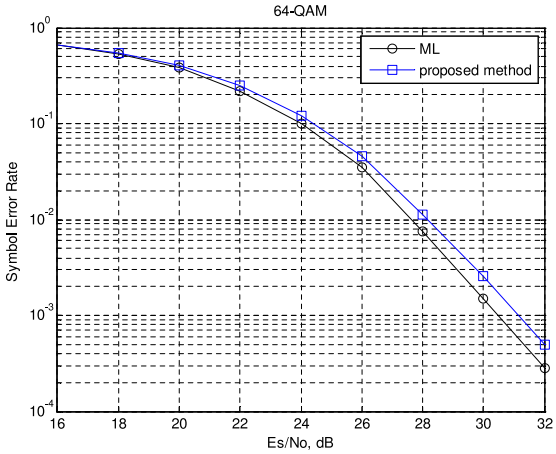

Fig. 2. A 4×4 sphere decoding using 64-QAM with K=7.

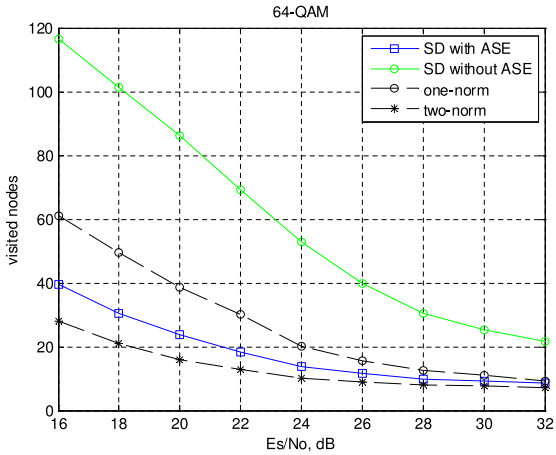

Fig. 3. The number of visited nodes as a function of SNR on 4×4 sphere decoding with and without ASE in 64-QAM.

The proposed ASE algorithm does greatly reduce the number of visiting nodes, which relates to the computational complexity, and this is shown in Fig. 3. The reduction is more than twice in a 4×4 MIMO system with 64-QAM.

B. VLSI Implementation

The schematic of the proposed 4×4 sphere decoder is as shown in Fig. 4, which contains the proposed ASE module, the MUL-free sphere ALU which evaluates (9), an LUT for

the proposed enumeration, and a controller to coordinate the control and data flow. To achieve 100 MHz system clock, we chose to use a TSMC 90 nm standard cell library for IC implementation. The fabricated die photo is shown in Fig. 5. Note that the MUL-free sphere ALU contains three sub-modules: C1 computes the b_{i+1} and C3 computes $R_{ii}s_i$ in (9) while C2 formulates the range in (10) by shifters and adders. Afterwards the ASE module performs the full function of (9). The target specification of the chip is summarized in Tab. II.

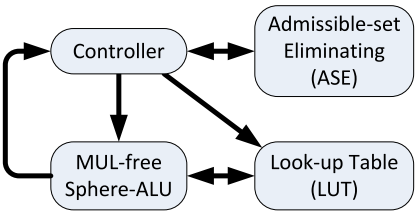

Fig. 4. The schematic of the proposed sphere decoder.

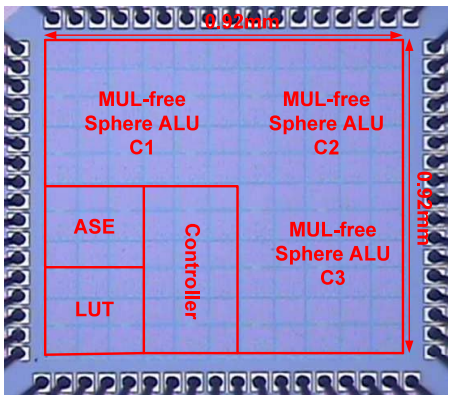

Fig. 5. The die photo of the proposed sphere decoder with sub-function annotation. The core dimension is 0.92 mm $\times$ 0.92 mm.

TABLE II

THE SPECIFICATION OF PROPOSED 4×4 SPHERE DECODER.

Items	Specification
Technology	TSMC 90 nm
Chip Area	2.386 mm^2
Core Area	0.855 mm^2
Gate Count	153.93 k
Max Frequency	108.69 MHz
Power Consumption	28.746 mW

With the proposed methods, the most immediate contribution is the throughput. Since the computations in each clock cycle do not involve direct multiplication or a long series of comparisons, the design can follow "one-node-per-cycle" scheduling. Assuming the system clock is at 100MHz, the average throughput of M-ary QAM is shown in Fig. 6 which shows that high data rate can be achieved using 64-QAM in high SNR region. Currently the fabricated chip is under testing for acquiring actual power consumption and throughput.

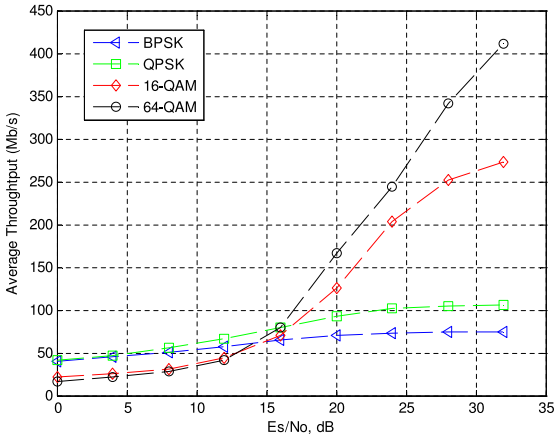

Fig. 6. The throughput of the proposed architecture for BPSK, QPSK, 16-QAM, and 64-QAM.

V. CONCLUSION

In this paper, we propose a table look-up enumeration method that partitions the surroundings of constellation points into 4 sub-regions for speedy K-best search. We also combine multiplier-free ASE to reduce the candidate nodes. Therefore, not only the chip area is reduced but also the critical paths are shortened. With concise computations the proposed sphere decoder can process one node at each clock cycle. Finally, the average throughput of the proposed architecture can achieve maximal throughput up to 411.3Mbps. Also the design supports BPSK, QPSK, 16-QAM, and 64-QAM modulations. The contribution can be more significant if the proposed methods are applied in higher M-ary QAM with more data streams.

ACKNOWLEDGMENT

We would like to thank the National Chip Implementation Center (CIC) for chip implementation and technical support.

REFERENCES

[1] W. Van Etten, "Maximum Likelihood Receiver for Multiple Channel Transmission Systems," *Communications, IEEE Transactions on*, vol.24, no.2, pp. 276-283, Feb 1976.

[2] Z. Guo and P. Nilsson, "Algorithm and Implementation of the K-best Sphere Decoding for MIMO Detection," *IEEE Journal on Selected Areas in Commu- nications*, vol. 24, no. 3, pp. 491-503, Mar. 2006.

[3] R. Shariat-Yazdi and T. Kwasniewski, "Configurable K-best MIMO Detector Architecture, in *Proc. 3rd International Symposium on Communications, Control and Signal Processing*, pp. 1565-1569, Mar. 2008.

[4] M. Wenk, M. Zellweger, A. Burg, N. Felber, and W. Fichtner, "K-best MIMO Detection VLSI Architectures Achieving up to 424 Mbps," in *Proc. IEEE International Symposium on Circuits and Systems*, pp.1151-1154, May 2006.

[5] A. Burg, M. Borgmann, M. Wenk, M. Zellweger, W. Fichtner, and H. Bolcskei, "VLSI Implementation of MIMO Detection Using the Sphere Decoding Algorithm," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1566-1577, Jul. 2005.

[6] C. Studer, A. Burg, and H. Bolcskei, "Soft-output Sphere Decoding: Algorithms and VLSI Implementation," *IEEE J. Sel. Areas Commun.*, vol. 26, no. 2, pp. 290-300, 2008.

[7] C. P. Schnorr and M. Euchner, "Lattice Basis Reduction: Improved Practical Algorithms and Solving Subset Sum Problems," *Math. Programming*, vol. 66, no 2, pp. 181-191, Sep. 1994.

[8] A. Wiesel, X. Mestre, A. Pages and J. R. Fonollosa, "Efficient implementation of sphere demodulation," *IEEE Workshop on Signal Processing Advances in Wireless Communications*, pp. 36-40, Jun. 2003.