Vehicular Signal Transmission Using Power Line Communications

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***Abstract*—We propose a power line communication (PLC) system for transmitting control signals in vehicle through internal power lines, such that the internal wires can be reduced and the vehicles can be lighter. The signals from different devices are multiplexed and modulated to the power lines by the transmitter. In the receiver, first the noise within power lines are filtered. Afterwards the multiplexed signals are selectively extracted by specific codes which are minimally correlated. Finally the control signals are restored from the error-control coded bits which make the information more robust. The maximum data rate of the chip is 50 $kbps$, and the die area is 3.74 mm^2 using a TSMC 0.18 μm standard cell library with power consumption 22.49 mW.**

I. Introduction

Power line communication (PLC) provides reliable broadband data transmission, and it is suitable for local area network deployment wherever power lines exist. In addition to fixed environment, mobile scenario such as vehicles are also filled with power lines. Recently electrical vehicles draw people's attention to achieve better fuel efficiency and environmental friendliness. Hundreds of sensors and control networks inside a car are expected to be essential, but the connected cables not only complicate the structure but also put on weight over a vehicle. When the weight of the vehicle increases, it also increases the fuel consumption. In [1], the authors pointed out that the weight of the cables for signalling cannot be neglected. Therefore, PLC may be a good solution for this case.

The requirements of signal quality and promptness for in-vehicle communication is different from that in general data communication system. The control signals such as stop lamps and break sensors must be transmitted and received accurately and immediately, because they are safety related. Unfortunately the wires of the vehicle are unavoidably corrupted with noise and crosstalk. Thus the performance would seriously degrade without careful transceiver design. The purpose of this research is to reduce the cost of the wire lines so that the weight of the vehicles can further be reduced. Here we apply PLC technology to build a communication system that can transmit the control signals over the power line in the vehicle as shown in Fig. 1. Several devices shares the same power line. To realize multiple signals transmitted by multiple components, the Gold codes are used to spread a bit into 31 chips. The corresponding control signals are encoded and spread respectively by the transmitter. Then the spread bits are modulated, converted by D/A, and then conveyed by the power line. The modulated signal in the power line is sampled by external A/D and fed into the receiver. The micro controller unit (MCU) selects the source of the modulated signal and the receiver decodes the corresponding data bits. For testing convenience, a pair of transmitter and receiver is integrated into a single chip using a TSMC $0.18\mu m$ process. The core area is $1.938mm \times 1.931mm$ (3.74 mm^2), and the power consumption is 22.49 mW at 40 Mhz operating frequency.

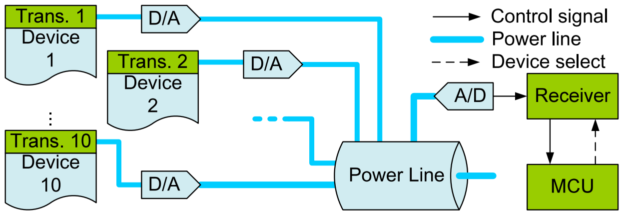

Fig. 1. System architecture.

Sec. II discusses system architecture. The proposed architecture is implemented and evaluated in Sec. III. The performance of the chip is presented in Sec. IV. Conclusions are provided in Sec. V.

II. System Architecture

The proposed system is able to support multi-users with low bit-error-rate. The target data rate from the sensors is 50kbps to save power consumption. This data rate is sufficient for control signal transmission. Fig. 2 shows how the baseband block diagram and the operational speed of the proposed system. The transmitter is composed by channel coding, spectrum spreading, and BPSK modulation. To fortify the signal integrity, error correction code is applied. Generally error correction code is categorized as block code and convolution code. In the proposed system block code is favored because its decoding latency is shorter than that of convolutional code. Prompt response is mandatory due to safety concern. Here Reed-Solomon (RS) code with code rate $1/3$ is applied in the proposed system. The data rate of the encoded codewords is therefore increased to 150kbps. The spectrum spreading uses 31-bit Gold sequence for multiplexing. This CDMA technique enables multiple devices transmit their signal simultaneously. 10 of the 31 Gold sequences are chosen so that the chosen sequences have the minimum correlation. Therefore, multiple devices can work concurrently with the minimum multiuser interference. After spectrum spreading the data rate becomes 4.65Mbps, and the data is modulated to power line in binary phase shift keying (BPSK). Finally, the modulated sequences

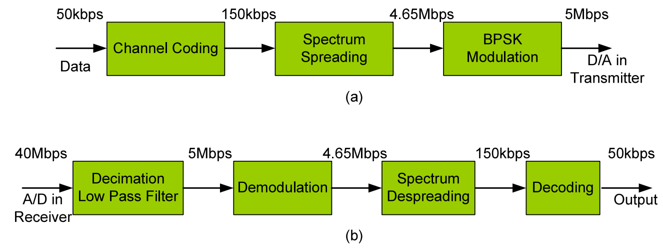

Fig. 2. The block diagram of baseband (a) transmitter and (b) receiver. The intermediate throughput and bandwidth are annotated.

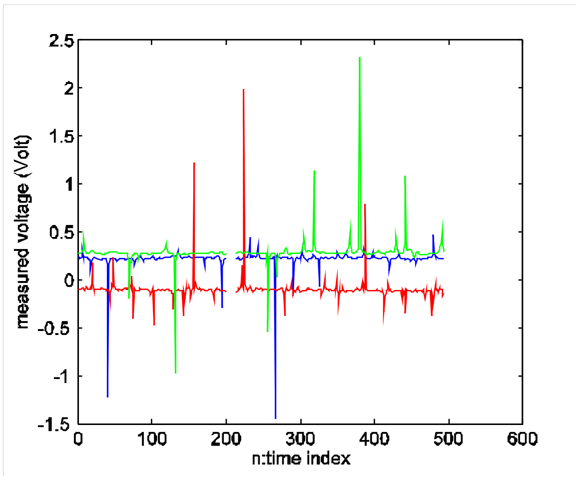

Fig. 3. Some measurements of spike noise and DC noise

are sent to the analog front end in the transmitter. At the receiver side, the received signal from the analog front end is assumed to have 12-bit resolution with sampling rate 40MHz to avoid aliasing. The details of the receiver functional blocks are delineated in the following sub-sections.

A. *RX Filter*

As all the communication channels induce interference, the power lines can also couple noise to corrupt the modulated information. To analyze the characteristics of the noise, we logged several typical noise patterns to analyze the corresponding characteristic. Some of the logged patterns are shown in Fig. 3, and the corresponding frequency spectrum is shown in Fig. 4. Fig. 3 shows that the interference contains spike noise and DC noise. Moreover, it is found that in addition to DC noise the spectrum of the interference is between 10MHz and 40MHz as shown in Fig. 4. Consequently, we suggest to use an ADC with 40 MHz sampling rate to avoid the aliasing of interference. The ADS800 from Texas Instruments (TI) satisfies the requirement [2].

Based on the spectrum in Fig. 4, we use two filters to mitigate two kinds of interference: one is the α filter, which is a first-order low-pass IIR filter to remove DC noise. Another filter is the decimation filter, which acts as a low-pass filter to cancel the interference above 10Mz. To match the 5MHz data rate at transmitter, the filtered samples are decimated by eight. Based on the above specification, we use Filterbuilder

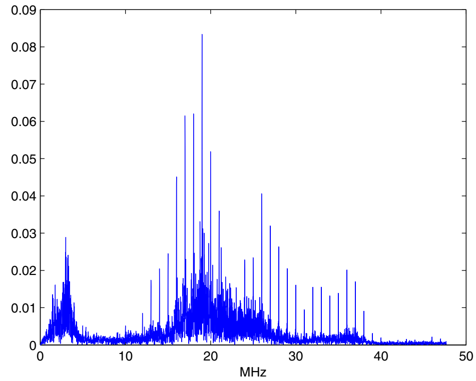

Fig. 4. Measured interference.

in Matlab to generate a 56 order low-pass filter with pass band at 8 MHz and stop band at 10MHz. Since the coefficients of the 56-tap filter are symmetric, only 28 constant multipliers are used.

B. *Spectrum Spreading/Despreading Using Gold Code*

We use CDMA to multiplex parallel bit streams. CDMA and OFDM are two of the most prevalent architectures for data multiplexing. However, each data stream in CDMA is designated with unique spread spectrum code which can be used as priority control. For example, both wiper blade and break send control signals at the same time. Each device has its own spread spectrum code such that the MCU can clearly distinguish the priority. In the proposed design we choose Gold code [3] because it has bounded low cross-correlation [4]. The property can help to perform individual synchronization in different pairs of transmitter and receiver when multiple devices are broadcasting in the same range.

Gold code is generated in two steps: First, two different bit sequence u and v are selected, which are of the same length $2^n - 1$. Second, the complete code set is generated as $\{u, v, u \oplus v, u \oplus Tv, u \oplus T^2 v, \ldots, u \oplus T^{2^n-2} v\}$, where T stands for one cyclic shift. Accordingly, Gold code can be generated by n-bit shift-register, which have $2^n + 1$ codes and each code has $2^n - 1$ bits. In the proposed design, we choose $n = 5$. The cross-correlation values for $n = 5$ are -1, -9, and 7. Here we choose 10 of the 31 spreading codes so that the chosen codes have cross-correlation value -1, and the corresponding encoder is as shown in Fig. 5. In the implementation, instead of using shift registers to generate the code set, the proposed design uses table-look-up to implement the Gold sequences.

The spectrum despreading in the receiver decodes one of the multiplexed control sequences selected by the MCU. Once the Gold code is chosen, the output of spectrum despreading uses exclusive-OR gate to compare the Gold code and received sequence.

C. *Reed-Solomon Codec*

Reed-Solomon code is the linear block code proposed by Reed and Solomon in 1960 [5]. RS code is popular in modern

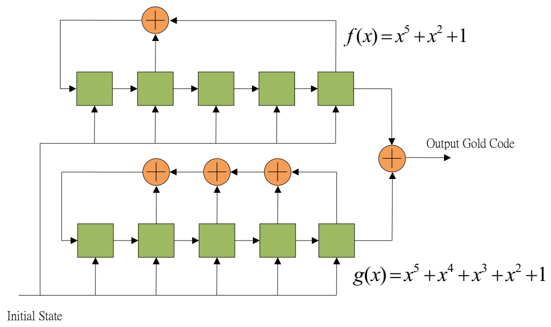

Fig. 5. The generation circuit of Gold code with $n = 5$

DSP applications because it is very effective in correcting random symbol errors and random burst errors. Conventionally the configuration of RS code is denoted as (n, k). n stands for the encoded codeword length while k is the word length before encoding. The length of parity check is $n - k$, and $t = \lfloor n - k/2 \rfloor$ errors can be corrected. In this work, the RS code configuration is $(15, 5)$.

Let α be a primitive element in $GF(q)$. $g(x)$ in Eq. (1) is the generator polynomial the RS code, where α, α^2, ..., α^{2t} are the roots of the generator polynomial.

$$g(x) = (x - \alpha)(x - \alpha^2) \cdots (x - \alpha^{2t}) \tag{1}$$

The generator polynomial of this work sets $t = 5$, and it is as shown in Eq. (2).

$$g(x) = x^{10} + \alpha^2 x^9 + \alpha^3 x^8 + \alpha^9 x^7 + \alpha^6 x^6 + \alpha^{14} x^5 + \alpha^2 x^4 + \alpha x^3 + \alpha^6 x^2 + \alpha x + \alpha^{10} \tag{2}$$

Let $I(x)$ be the information polynomial. The parity polynomial is derived by

$$I(x) \cdot x^{n-k} mod(g(x)) = p(x) \tag{3}$$

and the complete encoded code word polynomial of $\mathbf{C} = \{c_0, c_1, ..., c_{n-1}\}$ is

$$C(x) = I(x) \cdot x^{n-k} + p(x) \tag{4}$$

The RS encoder implemented in the proposed design is as shown in Fig. 6.

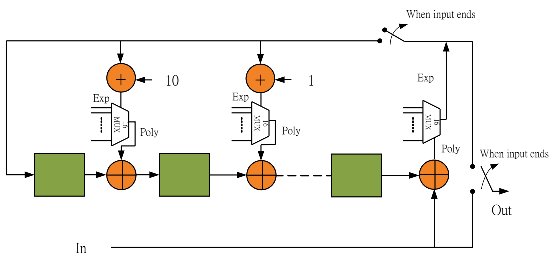

Fig. 6. The implementation of encoder in this work

Decoding RS code requires to determine both the error locations and the values of the received samples. The block diagram of a RS decoder is as shown in Fig. 7. The procedure

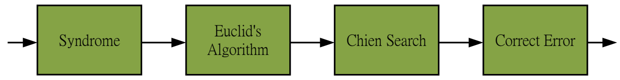

Fig. 7. The block diagram of a RS decoder

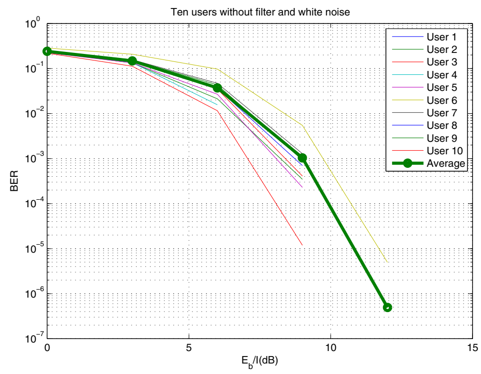

Fig. 8. The simulation of ten users without decimation filter

is as the following four steps [6]:

1) Compute the syndrome $\mathbf{S} = (S_1, S_2, \ldots, S_{2t})$.
2) Determine the error-location polynomial $\sigma(x)$ and error evaluation polynomial.
3) Evaluate error-location numbers by Chien search method.
4) Evaluate error-magnitudes and perform error correction.

The syndromes shall not be zero if there are errors. Based on the syndromes the error locator polynomial and error evaluation polynomial are derived by Euclidean Algorithm. Chien search pin point the error locations by substituting α_i into error locator polynomial. If the result is zero, i is the error location. Once the error location is found, the error value can be derived and hence the error in the received words can be corrected.

III. Evaluation of Proposed Architecture

The decimation filter in the receiver provides major performance enhancement. In Fig. 8 and Fig. 9, the system multiplexed the signals from 10 independent users (i.e. devices) without and with the decimation filter respectively. When the ratio of signal energy per bit over interference E_b/I is around 6 dB, the BER is 3×10^{-2} in the case without decimation filter while the BER is 3×10^{-7} in the case with decimation filter. Moreover, in the case with decimation filter, the BER is bounded at BER 10^{-7} once the (E_b/I) is larger than 6 dB. As to fix-point model evaluation in Fig. 9, the resolution of the word-length has been sufficiently reserved such that the difference between float-point model and fix-point model is not severe.

The number of users will affect the BER as well. The signal to one user is regarded as a kind of noise to the other users. The BER in the case of two users drops quicker than that of five users. In the case of two users when E_b/I is above 2dB, the information can fully be restored. Therefore the line for

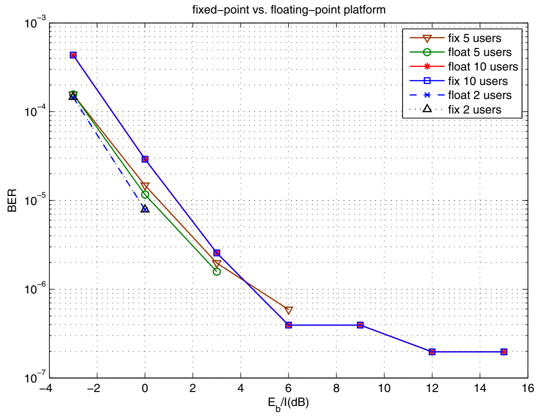

Fig. 9. The simulation of ten users with decimation filter;white noise with SNR = 1dB

Items	Specification
Technology	TSMC0.18um
Package	LCC68
Chip area	3.743 mm^2
Gate Count	109.62k
Max Frequency	40 MHz
Power Consumption (Estimated/Actual)	45/22.49 mW

TABLE I
SPECIFICATION OF THE PROPOSED PLC SYSTEM CHIP

two-user case is not continued in Fig. 9. As to the case of five users or more, even the added white-noise is 1 dB, the BER is still worse than 10^{-6} when the E_b/I is below 6dB. As the E_b/I gets better, the BER is improved accordingly.

IV. VLSI IMPLEMENTATION

The proposed system is designed to support 10 different devices, and the maximum data rate of each device is 50 kbps. The baseband system has been implemented into a single chip using a TSMC $0.18\mu m$ technology. Fig. 10 shows the photo and layout of the chip while the dimension and power consumption are as listed in Table I.

To verify the functionality of the chip, we have defined two kinds of test plan. One of the plans is using the multiplexed information generated by Matlab simulation. The patterns are fed into the chip by using Advantest V93000 PS1600 automatic test system. This test is abided by the testing procedure for commercial chip verification, and the actual power consumption and operating constraint can be acquired. The other test plan is to connect these chips for actual communication. Each chip serves one component. The encoded data from different chips are summed and fed into the receiver in another chip for decoding. The measured power consumption of the chips is 22.49mW on average. Since not all the functional blocks toggle at the same time, the power consumption from the synthesis report which accumulates the power of all the applied gates is larger than that of the fabricated chip in use.

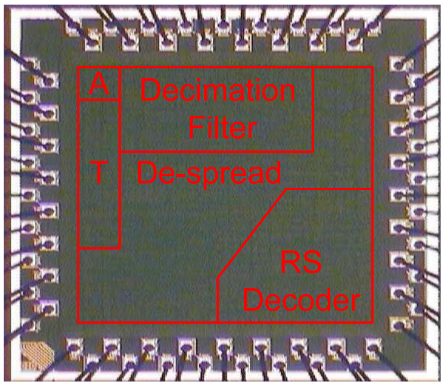

Fig. 10. The fabricated chip photo and the corresponding functional blocks. Area A is the α-filter and area T is the transmitter.

V. CONCLUSIONS

In this work we have proposed a PLC system to transmit the signal in vehicles over power line. By using the PLC with CDMA multiplexing method, we can reduce the consumption of wire lines. Furthermore we can increase the efficiency of the fuel. The system can support ten different devices and the maximal data rate of each component is 50 kbps. To mitigate the interference coupled by the power line, we use α filter and the decimation filter. The α filter removes DC noise, and the decimation filter mitigates the harmonic interference. Moreover we use RS code to combat the spike noise and guarantee the transmitting information is robust. From the system evaluation, the decimation filter significantly improves the BER. In hardware design, we replaced the Gold sequence generator by a table to decrease the encoding latency. In concurrent 10-user scenario with perfect synchronization, the BER of the system is less than 10^{-6} with SIR higher than 5 dB including SNR 1dB white noise. The chip has been taped out using a TSMC $0.18\mu m$ technology. The die area is 3.74 mm^2 and the measured power consumption is 22.49 mW on average under 40MHz operating frequency.

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